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FROM: Robert E. Scheid (Reg. No. 42,126)

DATE: July 19, 2005

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Contents of this Transmission:

Atty Docket No. 306812002500;

Inventor: David LEWIS et al.

Application No.: 10/057,232

Filing Date: January 25, 2002

Group Art Unit: 2825

Examiner: L. H. Malsawma

Title: SYSTEM AND METHOD FOR OPTIMIZING ROUTING LINES IN A

PROGRAMMABLE LOGIC DEVICE

Documents Filed:

Transmittal (1 page)

Request for Certificate of Correction (3 pages)

Certificate of Correction (1 page)

Sender's Initials:

RES4/Ixt4

Date

July 19, 2005

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)		Filing Date		January 25, 2002		
		First Named Inventor		David LEWIS		
		Art Unit		2825		
		Examiner Name		L. H. Malsawma		
Total Number of Pages in This Submission 5		sion 5	Attorney Docket Nurr	iber	306812002500	
ENCLOSURES (Check all that apply)						
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Fee A	Attached	Licensing-rel	ated Papers		Appeal Communication to Board of Appeals and Interferences	
Amendmen	Amendment/Reply Petition				Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)	
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Extension of Time Request Terminal Dis		claimer		Other Enclosure(s) (please Identify below):		
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Certified Copy of Priority Landscape Table on CD						
Reply to Missing Parts/ Remarks						
Reply 37 C	y to Missing Parts under FR 1.52 or 1.53					
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Firm Name MORRISON & FOERSTER LLP (Customer No. 20872)						
Signature Signature						
Printed name	Robert E. Scheid		·			
Date	July 19, 2005		Rag. No). (42,126	
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Dated: July 10,	2005 Signature:	(agus s		Lanus	Tsang)	

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JUL 1 9 2005

Docket No.: 306812002500

(PATENT)

Dated: July 19, 2005 Gigmetures (Laure Tsand)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:

David LEWIS et al.

Patent No.: 6,895,570 B2

Issued: May 17, 2005

For: SYSTEM AND METHOD FOR OPTIMIZING

ROUTING LINES IN A PROGRAMMABLE

LOGIC DEVICE

REQUEST FOR CERTIFICATE OF CORRECTION PURSUANT TO 37 CFR 1.322

Certificate of Correction Branch Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted typographical errors which should be corrected.

In the Claims:

In claim 9, line 8, please replace "inerconnects" with --interconnects--

In claim 11, line 3, please replace "horizonal" with --horizontal--

In claim 14, line 1, please replace "pogrammable" with -programmable-

In claim 19, line 10, please replace "pluality" with --plurality--

In claim 21, line 2, please replace "onsiderations" with -considerations-

Patent No.: 6,895,570 B2

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Docket No.: 306812002500

In claim 23, line 4, please replace "wires having first logical length" with --wires having a first logical length—

In claim 23, line 6, please replace "wires having a second logic length" with --wires having a second logical length--

In claim 23, line 28, please replace "length of the six subset" with --length of the sixth subset--

In claim 28, line 13, please replace "haing" with --having-

In claim 29, line 1, please replace "rchitecture" with -- architecture--

In claim 29, line 5, please replace "the fourth subset of the plurality of wires," with -the fourth subset of the plurality of wires,—

In claim 30, line 18, please replace "plurality of wires to the second starting point," with --plurality of wires at the second starting point,--

In claim 32, line 3, please replace "pluraity" with --plurality--

In claim 33, line 1, please replace "clim 23," with --claim 23,--

In claim 33, line 22, please replace "pllurality" with -plurality--

In claim 33, line 38, please replace "inlput' with --input--

In claim 33, line 46, please replace "of function block," with --of function blocks,-

In claim 40, line 1, please replace "of claim 5," with -of claim 35,--

JUL: 19. 2005 2:24PM MOFO 28TH FL NO. 283 P. 5

Patent No.: 6,895,570 B2

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Docket No.: 306812002500

In claim 44, line 8, please replace "a first one of the plurality of function blocks" with --a first one of the fourth subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks--

In claim 44, line 24, please replace "a third one of the plurality of function blocks" with -a third one of the second subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks—

In claim 45, line 25, please replace "pllurality" with --plurality-

The errors were not in the application as filed by applicant; accordingly no fee is required.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment.

Patentee respectfully solicits the granting of the requested Certificate of Correction.

In the unlikely event that the transmittal letter is separated from this document and/or the Patent Office determines that an extension and/or other relief is required, Applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to <u>Deposit</u>

Account No. 03-1952 referencing docket no. 306812002500.

Dated: July 19, 2005

Respectfully submitted,

Robert E. Scheid

Registration No.: 42,126 MORRISON & FOERSTER LLP

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PTO/SB44 (04-04)
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(Also Farm PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.

6,895,570 B2

DATED

May 17, 2005

INVENTOR(S)

David LEWIS et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims:

In claim 9, line 8, please replace "inerconnects" with --interconnects-

In claim 11, line 3, please replace "horizonal" with -horizontal-

In claim 14, line 1, please replace 'pogrammable' with -programmable-

In claim 19, line 2, please replace "pluality" with -plurality-

In claim 21, line 2, please replace "onsiderations" with -considerations-

In claim 23, line 4, please replace "wires having first logical length" with --wires having a first logical length--

in claim 23, line 6, please replace "wires having a second logic length" with —wires having a second logical length—

In claim 23, line 28, please replace "length of the six subset" with -length of the sixth subset-

In claim 28, fine 13, please replace "haing" with -having-

In claim 29, line 1, please replace "rchilecture" with -architecture-

In claim 29, line 5, please replace "the fourth subset of ythe plurality of wires," with -the fourth subset of the plurality of wires,-

In claim 30, line 18, please replace "plurality of wires to the second starting point," with --plurality of wires at the second starting point,--

In claim 32, line 3, please replace "plurafty" with --plurality--

In claim 33, line 1, please replace "clim 23," with -- claim 23,-

In claim 33, line 22, please replace "pilurality" with -pturality--

In claim 33, line 38, please replace "Inlput" with -Input-

In claim 33, line 48, please replace "of function block," with -of function blocks,-

in claim 40, line 1, please replace "of claim 5," with -of claim 35,-

In claim 44, line 8, please replace "a first one of the plurelity of function blocks" with —a first one of the fourth subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks—

In claim 44, line 24, please replace "a third one of the plurality of function blocks" with —a third one of the second aubset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks—

In claim 45, line 25, please replace "pilurality" with --plurality-

MAILING ADDRESS OF SENDER:

Robert E. Scheid

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8an Francisco, California 94105-2482

PATENT NO. 6,895,570 B2

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